ABSTRACT

Circuits, architectures, systems and methods for facilitating data communications and/or reducing latency in data communications. The architecture includes a clock recovery loop receiving data from a host device and providing a recovered clock signal, a filter circuit receiving recovered clock signal information and providing a control signal that adjusts the transmitter clock in response to recovered clock signal information and the two clock signals, and a transmitter receiving the control signal and transmitting data to a destination device in accordance with the transmitter clock. The circuitry generally includes a clock alignment block receiving first and second periodic signals and providing a control signal in response thereto, a filter for first periodic signal information, and a logic circuit configured to combine the control signal and the filtered information, thereby providing an adjustment signal for the second periodic signal. The systems generally relate to those that include the present architecture and/or circuit. The method generally includes determining a phase difference between first and second periodic signals, one of the periodic signals being recovered from a data stream; adjusting the other periodic signal in response to the phase difference and filtered information from the recovered periodic signal; and transmitting the data stream in accordance with said adjusted periodic signal. The present invention advantageously eliminates a FIFO memory in the data path, thereby reducing transceiver latency and improving system performance.